PCMCIA / JEIDA SRAM Card

Product Specification

Version 9

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Document Version

Version	Description	Date	Editor	Approved by
8	Update	2, April, 2002	Greg Lin	Greg Lin
9	Update	10, Aug., 2010	Amos Chung	Kent Liu

Contents

1 Introduction

1.1 General Description

Pretec high performance SRAM cards conform to the PCMCIA / JEIDA international standard and consist of multiple very low power consumption CMOS SRAM ICs, decoder IC and power control IC mounted on a very thin printed circuit board using surface mounting technology.

With the dual back-up battery design, each SRAM card contains a replaceable but non-rechargeable 3V lithium battery (main battery) and an on-board rechargeable but non-replaceable battery (auxiliary battery) for data retention. This design allows replacement of main battery without data loss for 20 minutes approximately. Digital signals on the BVD1*/BVD2* pins were used to alarm the user whether the main battery should be replaced to prevent the stored data from loss. With the flexible and user-friendly design, both BR2325 and CR2025 can be used as main battery. There is battery case lock system to prevent battery dropping from the card. Also, with the write-protect switch design, data will not be written into the card by accident.

Memory card attribute information represents various attribute information of a card and is stored at EVEN address of an attribute memory space which is enabled by asserting REG* signal. Regarding to the attribute information format, please refer to the PCMCIA 2.0 or JEIDA 4.1 specification. With the flexible design of this series cards, they provide 8K bytes E2PROM available for attribute memory or there is no attribute memory.

1.2 Features

- Interface: PCMCIA / JEIDA standard
- Capacity: 256K bytes ~ 8M bytes
- Data bus selectable: Byte (x8) / word (x16)
- Built-in write protect switch
- Credit card size: 54.0 x 85.6 x 3.3 (mm)
- Fast access time: 120ns (maximum)
- Attribute memory: 8 KB (optional 2KB/0KB by special request)
- Single +5V operating voltage
- Connector type: 2-piece, 2-row, 68 pins
- Battery:
  - Dual back-up battery design
  - Both BR2325 and CR2025 used as main battery
  - Battery voltage detection function
  - Battery case lock system

1.3 Product Number Definition

X1 X2 X3 X4X5X6 - X7

SRAM CARD (X1)

S: SRAM

A/M (Attribute Memory) (X2)

N: No A/M

A: With 2KB Read/Write A/M

6: With 8KB Read/Write A/M

Operating Voltage (X3)

5: 5V

Memory Capacity (X4X5X6)

256: 256KB

512: 512KB

001: 1MB

002: 2MB

004: 4MB

006: 6MB

008: 8MB

Extended Temperature (X7)

I (Industrial): -20°C ~ +85°C

E (Extended): -40°C ~ +85°C

Note: A/M means attribute memory

1.4 Ordering Information

(Industrial grade: -20°C ~ +85°C)

Item No.	Part Number	Capacity	Attribute Memory	Description
1	SA5256-I	256KB	2KB E^2PROM	256KB 2KB A/M SRAM Card
2	SA5512-I	512KB		512KB 2KB A/M SRAM Card
3	SA5001-I	1MB		1MB 2KB A/M SRAM Card
4	SA5002-I	2MB		2MB 2KB A/M SRAM Card
5	SA5004-I	4MB		4MB 2KB A/M SRAM Card
6	SA5006-I	6MB		6MB 2KB A/M SRAM Card
7	SA5008-I	8MB		8MB 2KB A/M SRAM Card
8	S65256-I	256KB	8KB E^2PROM	256KB 8KB A/M SRAM Card
9	S65512-I	512KB		512KB 8KB A/M SRAM Card
10	S65001-I	1MB		1MB 8KB A/M SRAM Card
11	S65002-I	2MB		2MB 8KB A/M SRAM Card
12	S65004-I	4MB		4MB 8KB A/M SRAM Card
13	S65006-I	6MB		6MB 8KB A/M SRAM Card
14	S65008-I	8MB		8MB 8KB A/M SRAM Card
15	SN5256-I	256KB	None	256KB no A/M SRAM Card
16	SN5512-I	512KB		512KB no A/M SRAM Card
17	SN5001-I	1MB		1MB no A/M SRAM Card
18	SN5002-I	2MB		2MB no A/M SRAM Card
19	SN5004-I	4MB		4MB no A/M SRAM Card
20	SN5006-I	6MB		6MB no A/M SRAM Card
21	SN5008-I	8MB		8MB no A/M SRAM Card

(Extended grade: -40°C ~ +85°C)

Item No.	Part Number	Capacity	Attribute Memory	Description
1	SA5256-E	256KB	2KB E^2PROM	256KB 2KB A/M SRAM Card
2	SA5512-E	512KB		512KB 2KB A/M SRAM Card
3	SA5001-E	1MB		1MB 2KB A/M SRAM Card
4	SA5002-E	2MB		2MB 2KB A/M SRAM Card
5	SA5004-E	4MB		4MB 2KB A/M SRAM Card
6	SA5006-E	6MB		6MB 2KB A/M SRAM Card
7	SA5008-E	8MB		8MB 2KB A/M SRAM Card
8	S65256-E	256KB	8KB E^2PROM	256KB 8KB A/M SRAM Card
9	S65512-E	512KB		512KB 8KB A/M SRAM Card
10	S65001-E	1MB		1MB 8KB A/M SRAM Card
11	S65002-E	2MB		2MB 8KB A/M SRAM Card
12	S65004-E	4MB		4MB 8KB A/M SRAM Card
13	S65006-E	6MB		6MB 8KB A/M SRAM Card
14	S65008-E	8MB		8MB 8KB A/M SRAM Card
15	SN5256-E	256KB	None	256KB no A/M SRAM Card
16	SN5512-E	512KB		512KB no A/M SRAM Card
17	SN5001-E	1MB		1MB no A/M SRAM Card
18	SN5002-E	2MB		2MB no A/M SRAM Card
19	SN5004-E	4MB		4MB no A/M SRAM Card
20	SN5006-E	6MB		6MB no A/M SRAM Card
21	SN5008-E	8MB		8MB no A/M SRAM Card

2 Product Specification

2.1 Pin Configuration

Pin No.	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
Pin Name	GND	D3	D4	D5	D6	D7	CE1*	A10	OE*	A11	A9	A8	A13
Pin No.	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**
Pin Name	A14	WE*	BUSY*	VCC	VPP1	A16	A15	A12	A7	A6	A5	A4	A3
Pin No.	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**
Pin Name	A2	A1	A0	D0	D1	D2	WP	GND	GND	CD1*	D11	D12	D13
Pin No.	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	**48**	**49**	**50**	**51**	**52**
Pin Name	D14	D15	CE2*	VS1*	NC	NC	A17	A18	A19	A20	A21	VCC	VPP2
Pin No.	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	**62**	**63**	**64**	**65**
Pin Name	A22	A23	A24	A25	VS2*	RESET	WAIT*	NC	REG*	BVD2*	BVD1*	D8	D9
Pin No.	**66**	**67**	**68**										
Pin Name	D10	CD2*	GND										

Note: * mean low active

VPP1, VPP2, A23, A24, A25, RESET, WAIT* is NC

CD1*, CD2* connected to ground

2.2 Pin Description

Symbol	Function	I/O
A0 - A23	Addresses	I
D0 - D15	Data Inputs/Outputs	I/O
CE1*/CE2*	Card Enable	I
OE*	Output Enable	I
WE*	Write Enable	I
REG*	Attribute Memory Enable	I
WP	Write-protect Detect	O
BVD1*/BVD2*	Battery Voltage Detect	O
BUSY*	Busy Output (Open drain)	O
CD1*/CD2*	Card Detect (tied to GND internally)	O
VCC	+5 Volt Power Supply (3.3Volt optional)	-
GND	Ground	-
NC	No Connection	-

Note: * mean low active

2.3 Block Diagram

(256KB - 8MB SRAM Card)

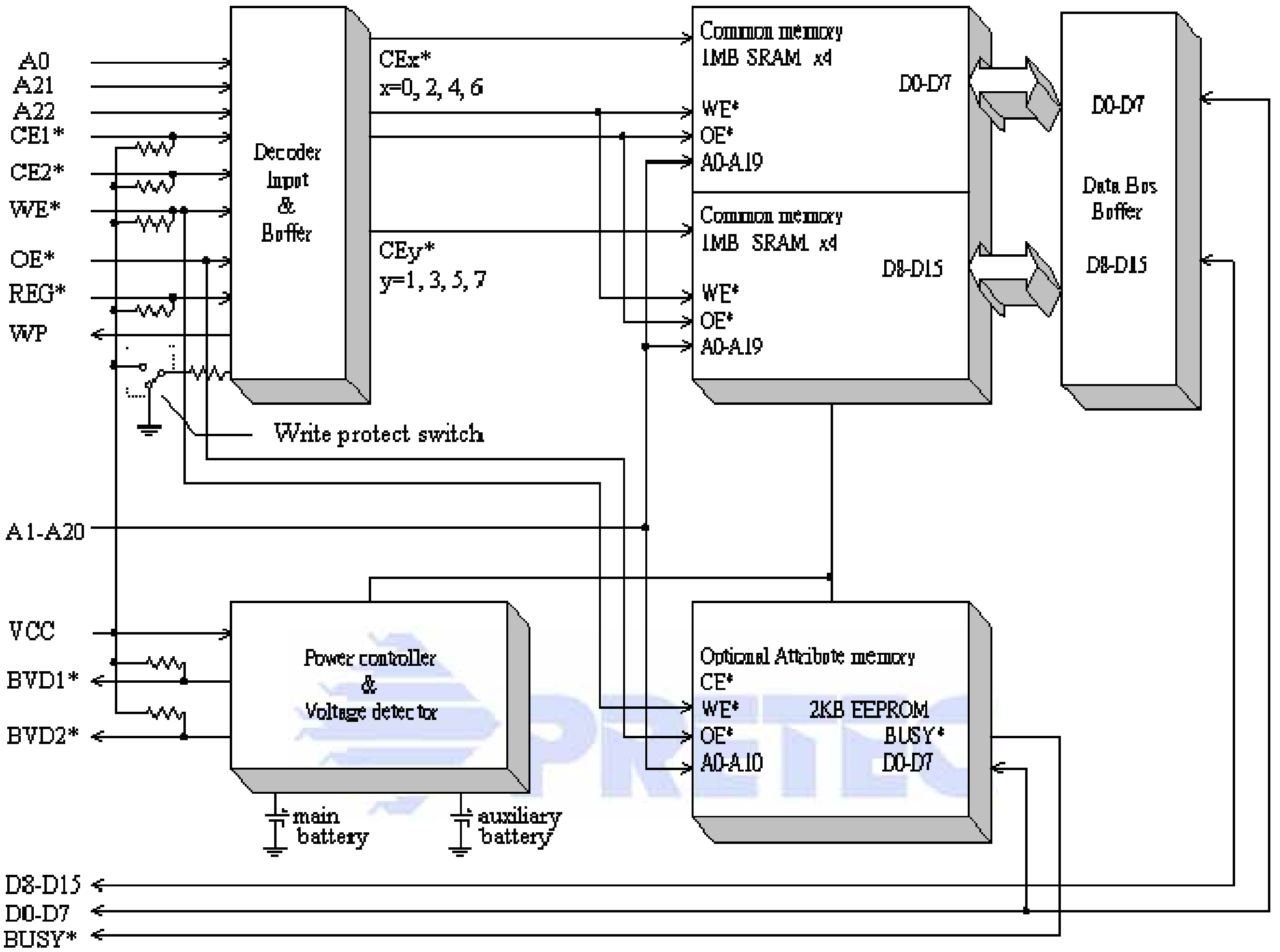


Figure 1: The Block Diagram of SRAM Card

Note: A0, A21, A22 are chip decoding address pins.

2.4 Pin Location

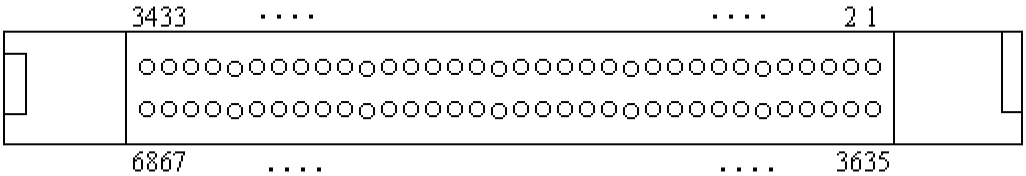


Figure 2: Bottom View (Connector Side)

2.5 Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VCC	4.5	5.5	V
Input High Voltage	VIH	0.7VCC	VCC + 0.3	V
Input Low Voltage	VIL	- 0.3	0.8	V
Battery Voltage	VBAT	2.37	-	V
Operating Temperature (Commercial)	TOPR	0	60	C
Operating Temperature (Industrial)	TOPR	-40	85	C
Relative Humidity (non-condensing)	HUM	-	95	%

2.6 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to + 6.0	V
Input Voltage	VIN	-0.5 to VCC + 0.3 (6V max.)	V
Output Voltage	VOUT	-0.5 to + 6.0	V
Operating Temperature (Commercial)	TOPR	-10 to + 70	C
Storage Temperature (Commercial)	TSTR	-20 to + 70	C
Operating Temperature (Industrial)	TOPR	-40 to + 85	C
Storage Temperature (Industrial)	TSTR	-40 to + 85	C
Relative Humidity (non-condensing)	HUM	95 (maximum)	%

2.7 Comments

Stress above those listed under “Absolute Maximum Ratings” may cause permanent damage to the products. These are stress rating only. Functional operation of these products at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

3 Product Model

3.1 Function without write protected

Function	REG*	CE2*	CE1*	A0	OE*	WE*	WP	D15 - D8	D7 - D0
Read C/M (x8)	H	H	L	L	L	H	L	High - Z	Even Byte Data Out
Read C/M (x8)	H	H	L	H	L	H	L	High - Z	Odd Byte Data Out
Read C/M (x8)	H	L	H	X	L	H	L	Odd Byte Data Out	High - Z
Read C/M (x16)	H	L	L	X	L	H	L	Odd Byte Data Out	Even Byte Data Out
Write C/M (x8)	H	H	L	L	H	L	L	X	Even Byte Data In
Write C/M (x8)	H	H	L	H	H	L	L	X	Odd Byte Data In
Write C/M (x8)	H	L	H	X	H	L	L	Odd Byte Data In	X
Write C/M (x16)	H	L	L	X	H	L	L	Odd Byte Data In	Even Byte Data In
Standby	X	H	H	X	X	X	L	High - Z	High - Z
Output Disable	X	X	X	X	H	H	L	High - Z	High - Z
Read A/M (x8)	L	H	L	L	L	H	L	High - Z	Even Byte Data Out
Read A/M (x8)	L	H	L	H	L	H	L	High - Z	Data Out (invalid)
Read A/M (x8)	L	L	H	X	L	H	L	Data Out (invalid)	High - Z
Read A/M (x16)	L	L	L	X	L	H	L	Data Out (invalid)	Even Byte Data Out
Write A/M (x8)	L	H	L	L	H	L	L	X	Even Byte Data In
Write A/M (x8)	L	H	L	H	H	L	L	X	X
Write A/M (x8)	L	L	H	X	H	L	L	X	X
Write A/M (x16)	L	L	L	X	H	L	L	X	Even Byte Data In

Note: * mean low active

3.2 Function with write protected

Function	REG*	CE2*	CE1*	A0	OE*	WE*	WP	D15 - D8	D7 - D0
Read C/M (x8)	H	H	L	L	L	H	H	High - Z	Even Byte Data Out
Read C/M (x8)	H	H	L	H	L	H	H	High - Z	Odd Byte Data Out
Read C/M (x8)	H	L	H	X	L	H	H	Odd Byte Data Out	High - Z

Read C/M (x16)	H	L	L	X	L	H	H	Odd Byte Data Out	Even Byte Data Out
Write C/M (x8)	H	H	L	L	H	L	H	X	X
Write C/M (x8)	H	H	L	H	H	L	H	X	X
Write C/M (x8)	H	L	H	X	H	L	H	X	X
Write C/M (x16)	H	L	L	X	H	L	H	X	X
Standby	X	H	H	X	X	X	H	High - Z	High - Z
Output Disable	X	X	X	X	H	H	H	High - Z	High - Z
Read A/M (x8)	L	H	L	L	L	H	H	High - Z	Even Byte Data Out
Read A/M (x8)	L	H	L	H	L	H	H	High - Z	Data Out (invalid)
Read A/M (x8)	L	L	H	X	L	H	H	Data Out (invalid)	High - Z
Read A/M (x16)	L	L	L	X	L	H	H	Data Out (invalid)	Even Byte Data Out
Write A/M (x8)	L	H	L	L	H	L	H	X	X
Write A/M (x8)	L	H	L	H	H	L	H	X	X
Write A/M (x8)	L	L	H	X	H	L	H	X	X
Write A/M (x16)	L	L	L	X	H	L	H	X	X

Note:

Definition: C/M = Common Memory, A/M = Attribute Memory

L = V_{IL}; H = V_{IH}; X = Don't care (can be either V_{IH} or V_{IL})

* mean low active

3.3 Common Memory Address Configuration

3.3.1 Using 8-bit Data Bus (CE2*=V_{IH}, CE1*=V_{IL})

A23 to A0	D15 -- D8	D7 -- D0
00 0000 0000 0000 0000 0000	High - Z	Address 0
00 0000 0000 0000 0000 0001	High - Z	Address 1
00 0000 0000 0000 0000 0010	High - Z	Address 2
11 1111 1111 1111 1111 1101	High - Z	Address 8388605
11 1111 1111 1111 1111 1110	High - Z	Address 8388606
11 1111 1111 1111 1111 1111	High - Z	Address 8388607

3.3.2 Using 8-bit Data Bus (CE2*=V_{IL}, CE1*=V_{IH})

A23 to A0	D15 -- D8	D7 -- D0
00 0000 0000 0000 0000 000X	Address 1	High - Z
00 0000 0000 0000 0000 001X	Address 3	High - Z
00 0000 0000 0000 0000 010X	Address 5	High - Z
11 1111 1111 1111 1111 101X	Address 8388603	High - Z
11 1111 1111 1111 1111 110X	Address 8388605	High - Z
11 1111 1111 1111 1111 111X	Address 8388607	High - Z

3.3.3 Using 16-bit Data Bus (CE2*=V_{IL}, CE1*=V_{IL})

A23 to A0	D15 -- D8	D7 -- D0
00 0000 0000 0000 0000 000X	Address 1	Address 0
00 0000 0000 0000 0000 001X	Address 3	Address 2
00 0000 0000 0000 0000 010X	Address 5	Address 4
11 1111 1111 1111 1111 101X	Address 8388603	Address 8388602
11 1111 1111 1111 1111 110X	Address 8388605	Address 8388604
11 1111 1111 1111 1111 111X	Address 8388607	Address 8388606

Note:

The above tables are examples for 8M bytes / 4M words SRAM cards.

Definition: L = V_{IL}; H = V_{IH}; X = Don’t care (can be either V_{IH} or V_{IL})

3.4 DC Electrical Characteristic

Symbol	Parameter	-	Min.	Max.	Unit	Test Conditions
I_{LI}	Input Leakage Current	-	-10	10	uA	V_{IN} = 0V to Vcc (Note 3)
			-70	10	uA	V_{IN} = 0V to Vcc (Note 4)
I_{LO}	Output Leakage Current	-	-10	10	uA	CE1* = CE2* = V_{IH} or OE* = V_{IH}, $V_{I/O}$ = 0V to Vcc (Note 1)
V_{OH}	Output High Voltage	-	3.8	-	V	I_{OH} = -2mA (Note 2)
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 3.2mA (Note 2)
V_{IH}	Input High Voltage	-	0.7Vcc	Vcc+0.3	V	-
V_{IL}	Input Low Voltage	-	-0.3	0.3Vcc	V	-
I_{CC}	Vcc Operating Current	-	-	120	mA	Min. cycle, I_{Out} = 0mA
I_{SB}	Vcc Standby Current (CE1* = CE2* = VIH or CE1* = CE2 * VCC - 0.2V)	-	-	0.1	mA	For page 7 & 8, item 15
				0.2	mA	For page 7 & 8, item 16
				0.1	mA	For page 7 & 8, item 17
				0.2	mA	For page 7 & 8, item 18

				0.3	mA	For page 7 & 8, item 19
				0.3	mA	For page 7 & 8, item 20
				0.35	mA	For page 7 & 8, item 21
				0.15	mA	For page 7 & 8, item 1 & 8
				0.25	mA	For page 7 & 8, item 2 & 9
				0.15	mA	For page 7 & 8, item 3 & 10
				0.25	mA	For page 7 & 8, item 4 & 11
				0.35	mA	For page 7 & 8, item 5 & 12
				0.35	mA	For page 7 & 8, item 6 & 13
				0.4	mA	For page 7 & 8, item 7 & 14
IBU	Battery Back-up Current (All pins open, VBAT = 3V Vcc = 0V)	256KB	-	40	uA	1uA (Ta = 25°C)
		512KB	-	80	uA	2uA (Ta = 25°C)
		1MB	-	50	uA	1uA (Ta = 25°C)
		2MB	-	100	uA	2uA (Ta = 25°C)
		4MB	-	200	uA	4uA (Ta = 25°C)
		6MB	-	160	uA	4uA (Ta = 25°C)
		8MB	-	400	uA	8uA (Ta = 25°C)
VBDET1	Battery Detect Reference Voltage 1		2.27	2.47	V	2.37V (Typ.) Vcc = 5V, Ta = 25°C
VBDET2	Battery Detect Reference Voltage 2		2.55	2.75	V	2.65V (Typ.) Vcc = 5V, Ta = 25°C

Note:

1. Except BVD1*, BVD2*, CD1*, CD2* pins
2. Except CD1*, CD2* pins
3. Except CE1*, CE2*, WE*, REG* pins
4. For CE1*, CE2*, WE*, REG* pins

3.5 AC Electrical Characteristics (Common Memory)

3.5.1 Read Cycle

Symbol	Parameter	Min.	Max.	Unit
tcr	Read Cycle Time	120	-	ns
ta(A)	Address Access Time	-	120	ns
ta(CE)	Card Enable Access Time	-	120	ns
ta(OE)	Output Enable Access Time	-	60	ns
tdis(CE)	Output Disable Time (CE*)	-	60	ns
tdis(OE)	Output Disable Time (OE*)	-	60	ns
ten(CE)	Output Enable Time (CE*)	5	-	ns
ten(OE)	Output Enable Time (OE*)	5	-	ns
tv(A)	Data Hold Time (from address changed)	0	-	ns

3.5.2 Write Cycle

Symbol	Parameter	Min.	Max	Unit
tcw	Write Cycle Time	120	-	ns
tw(WE)	Write Pulse Width	80	-	ns
tsu(A)	Address Setup Time	20	-	ns
tsu(A-WEH)	Address Setup Time (WE*)	100	-	ns
tsu(CE-WEH)	CE* Setup Time (WE*)	100	-	ns
tsu(D-WEH)	Data Setup Time (WE*)	50	-	ns
th(D)	Data Hold Time	20	-	ns
trec(WE)	Write Recovery Time	20	-	ns
tdis(WE)	Output Disable Time (WE*)	-	60	ns
tdis(OE)	Output Disable Time (OE*)	-	60	ns
ten(WE)	Output Enable Time (WE*)	5	-	ns
ten(OE)	Output Enable Time (OE*)	5	-	ns
ten(OE-WE)	Output Enable Setup Time (WE*)	10	-	ns
th(OE-WE)	Output Enable Hold Time (WE*)	10	-	ns

3.5.3 Test Conditions

Input Pulse Level	V_{OH} = 0.7Vcc , V_{IL}= 0.8V
Input Rise and Fall Time	5ns (max)
Timing Measurement Reference Level	V_{IH} / V_{IL} = 2.4V / 0.6V , V_{OH} / V_{OL} = 2V / 0.8V
Output Load	1TTL Gate + 100PF (Figure 3)

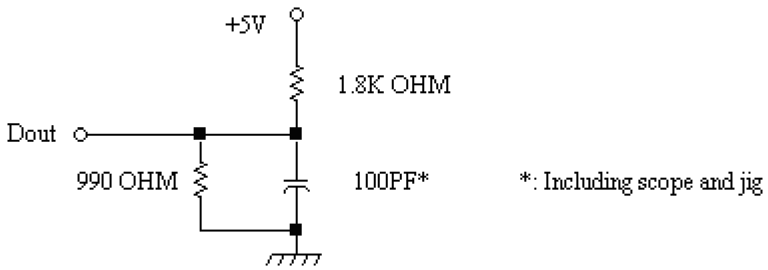


Figure 3: The Test Conditions of AC Characteristics

3.5.4 Input / Output Capacitance

(Ta = 25°C, f = 1MHZ, Vin/Vout = 0V), these parameters are sampled not 100% tested.

Symbol	Parameter	Min.	Max.	Unit
Cin	Input Capacitance	-	110	PF
Ci/o	I/O Capacitance	-	35	PF

3.5.5 Timing Diagram

Read Cycle (WE*=REG*=V_{IH})

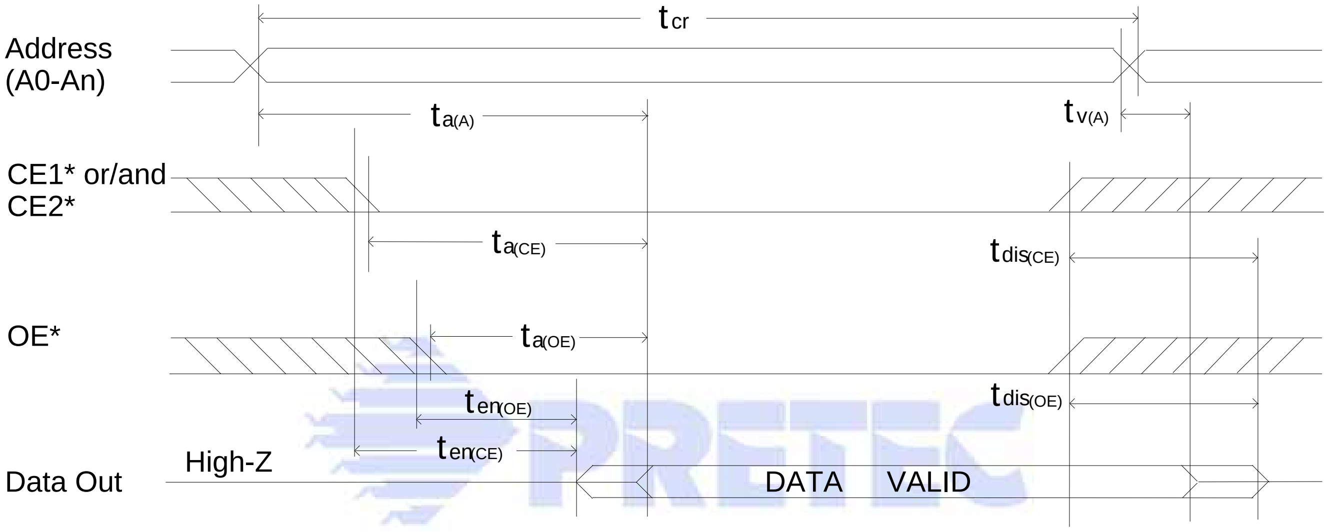


Figure 4: The Timing Diagram of Read Cycle (Common Memory)

Note:

1. For 64KB, An = A15. 128KB, An = A16. 256KB, An = A17. 512KB, An = A18.
   1MB, An = A19. 2MB, An = A20. 4MB, An = A21 6MB, An = A22.
2. The shaded area may be either high or low.

Write Cycle (REG*=V_{IH}, WE* controlled)

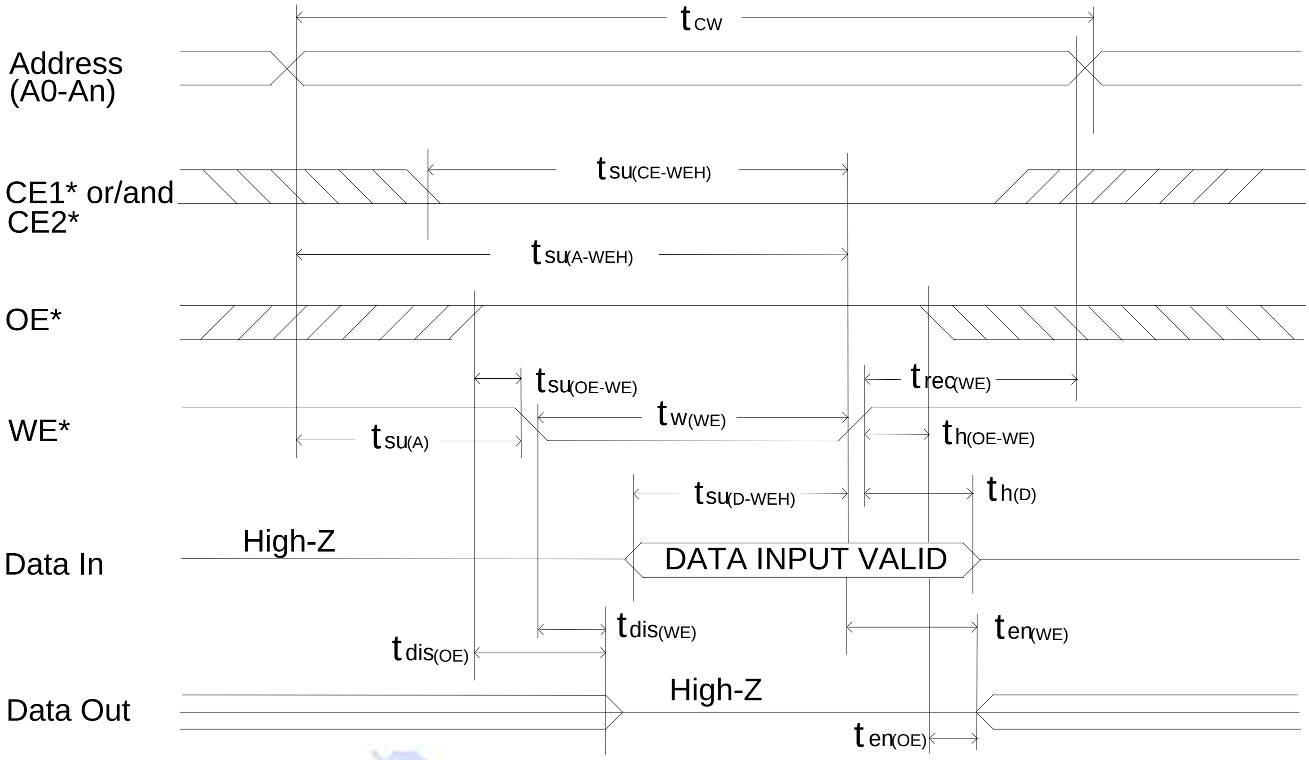


Figure 5: The Timing Diagram of Write Cycle (REG=VIH, WE* controlled) (Common Memory)*

Write Cycle (CE* controlled, OE*=REG*=V_{IH})

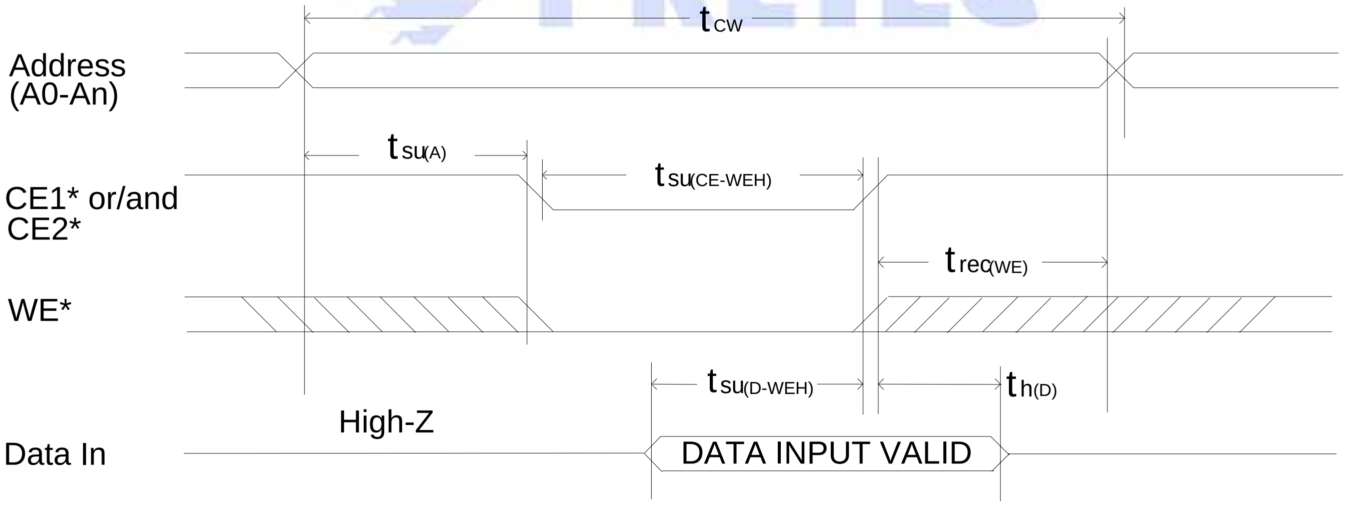


Figure 6: The Timing Diagram of Write Cycle (CE controlled, OE*=REG*=VIH)*

Note:

1. For 64KB, An = A15. 128KB, An = A16. 256KB, An = A17. 512KB, An = A18.
   1MB, An = A19. 2MB, An = A20. 4MB, An = A21 6MB, An = A22.
2. The shaded area may be either high or low.

3.6 AC Electrical Characteristics (Attribute Memory)

3.6.1 Read Cycle

Symbol	Parameter	Min.	Max	Unit
tcr	Read Cycle Time	300	-	ns
ta(A)	Address Access Time	-	300	ns
ta(CE)	Card Select Access Time	-	300	ns
ta(OE)	Output Enable Access Time	-	150	ns
tdis(CE)	Output Disable Time (from CE*)	-	100	ns
tdis(OE)	Output Disable Time (from OE*)	-	100	ns
ten(CE)	Output Enable Time (from CE*)	5	-	ns
ten(OE)	Output Enable Time (from OE*)	5	-	ns
tv(A)	Data Hold Time (from address changed)	0	-	ns

3.6.2 Write Cycle

Symbol	Parameter	Min.	Max.	Unit
tcw	Write Cycle Time	-	1	ms
tAS	Address Setup Time	30	-	ns
tAH	Address Hold Time	50	-	ns
tWP	Write Pulse Width	120	-	ns
tCS	Card Enable Time to WE*	15	-	ns
tCH	Card Enable Hold Time from WE* High	0	-	ns
tDS	Data Setup Time	70	-	ns
tDH	Data Hold Time	30	-	ns
tOES	OE* Setup Time	30	-	ns
tOEH	OE* Hold Time	30	-	ns
tDB	Delay from WE* high to BUSY* Asserted	-	50	ns

3.6.3 Timing Diagram

Read Cycle (REG*=VIL , WE*=VIH)

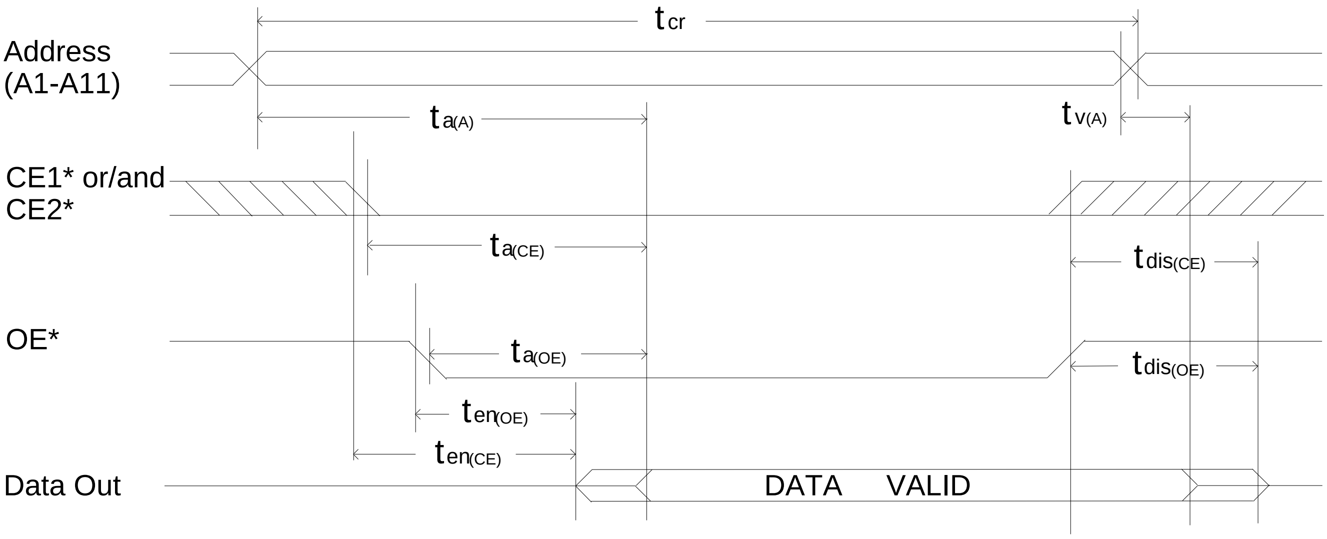


Figure 7: The Timing Diagram of Read Cycle (Attribute Memory)

Write Cycle (REG*=VIL)

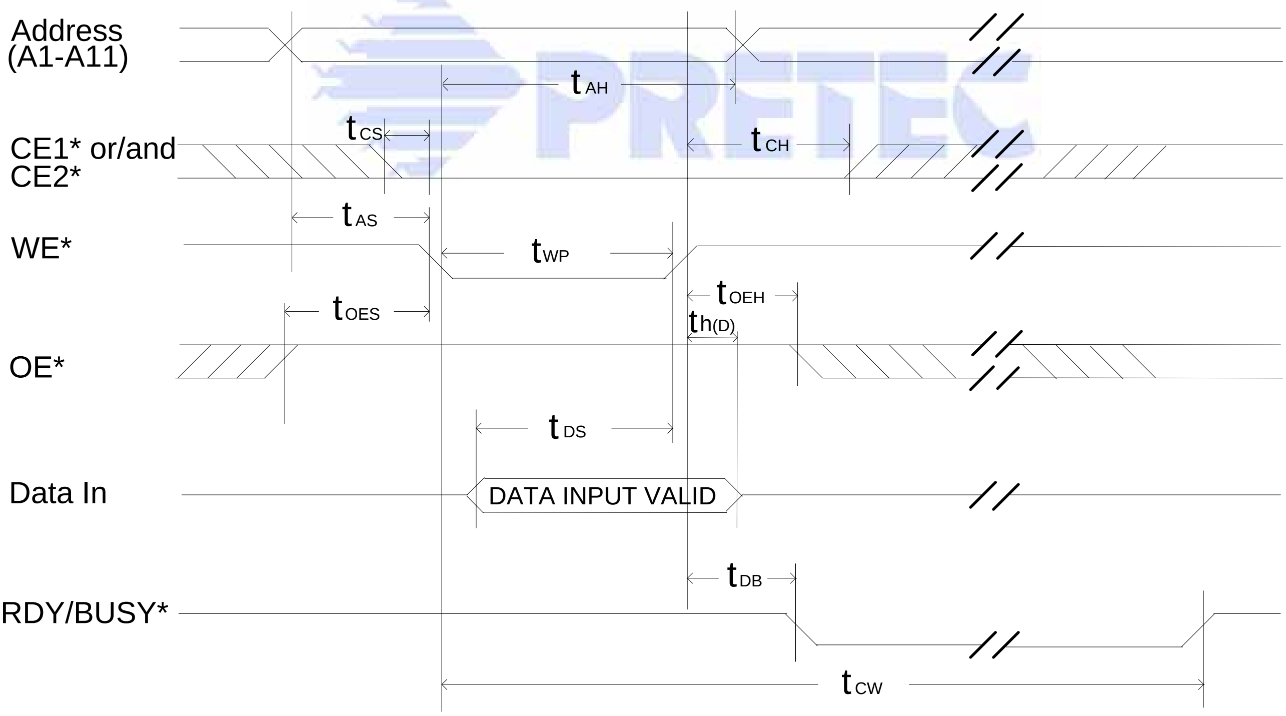


Figure 8: The Timing Diagram of Write Cycle (Attribute Memory)

3.6.4 Battery Voltage Detection

BVD1*/BVD2* pins are used to monitor the voltage of the main battery which should be maintained at 2.65V or greater for data retention. The following table described the main battery status by reading the signals on BVD1*/BVD2* pins.

BVD1*	BVD2*	Main Battery	Comments
H	H	VBAT 2.65V	Data retention is OK. Battery is operational
H	L	2.37V < VBAT < 2.65V	Data retention is OK. But battery should be replaced.
L	L	VBAT < 2.37V	Data integrity is not guaranteed. Battery must be replaced.

Note: if the main battery is removed, BVD1* and BVD2* pins will not function

3.7 Main Battery Specifications

3V Lithium battery

Diameter	Thickness	Brand	Model No.
23.0mm	2.5mm	RAYOVAC	BR2325
		FDK	CR2325
		PANASONIC	BR2325

Recommended parts (Please refer to the table below)

Diameter	Thickness	Brand	Model No.
20.0mm	2.5mm	TOSHIBA	CR2025
		FDK	CR2025
		PANASONIC	CR2025

3.7.1 Approximate Battery Life Time under Battery Back-up only

(Ta=25°C, Humidity=60% R.H.)

unit: year

Product Part No.	Battery Life
SA5256C, SA5256E	6 / 4.5
SA5512C, SA5512E	4 / 3
SA5001C, SA5001E	6 / 4.5
SA5002C, SA5002E	4 / 3
SA5004C, SA5004E	2.5 / 2
SA5006C, SA5006E	2.5 / 2

Product Part No.	Battery Life
SN5256C, SN5256E	6 / 4.5
SN5512C, SA5512E	4 / 3
SN5001C, SA5002E	6 / 4.5
SN5002C, SN5002E	4 / 3
SN5004C, SN5004E	2.5 / 2
SN5006C, SN5006E	2.5 / 2

Note:

For battery life, the numbers on the left-hand side of slash denote using 2325 series batteries. The numbers on the right-hand side of slash denote using 2025 series batteries.

3.8 Card Detection

CD1*, CD2* pins are used to detect the insertion of the card into the system. When the memory card has been correctly inserted, CD1* and CD2* are detected by the system. The recommended circuit in the system side is shown in figure below.

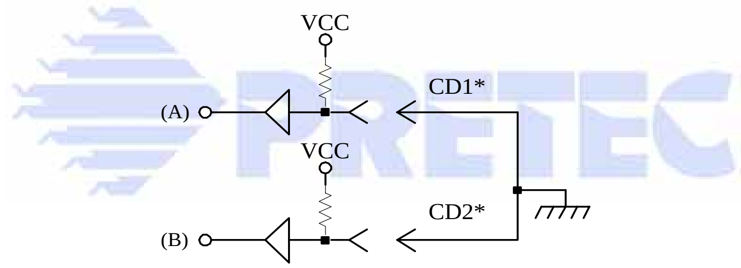


Figure 9: The Card Detection

3.9 Power-up / Power-down Characteristics

Symbol	Parameter	Min.	Max.	Unit	Condition
Vi(CE)	CE* Signal Level	0	ViMAX[*1]	V	0V VCC < 2.0[*2]
		VCC-0.1	ViMAX	V	2.0 VCC < VIH
		V_{IH}	ViMAX	V	VIH VCC
tsu(VCC)	CE* Setup Time	20	-	ms	10ms (Typ.)
trec(VCC)	CE* Recovery Time	1	-	us	-
Tpr[*3]	VCC Rising Time	0.1	300	ms	10% 90% (VCC+5%)
Tpf[*3]	VCC Falling Time	3.0	300	ms	90% (VCC-5%) 10%

Note:

1. ViMAX means absolute maximum voltage for input.
2. For the period 0V VCC< 2.0V, power supply voltage is low, so 0V~ ViMAX is permitted,

because the logic for the system interface IC may not be determined.

3. The Tpr and Tpf are defined as "linear waveform" in the period of 10% to 90%. Even if the waveform is not "linear waveform", its rising and falling time must meet this specification.

3.9.1 Power-up Timing Diagram

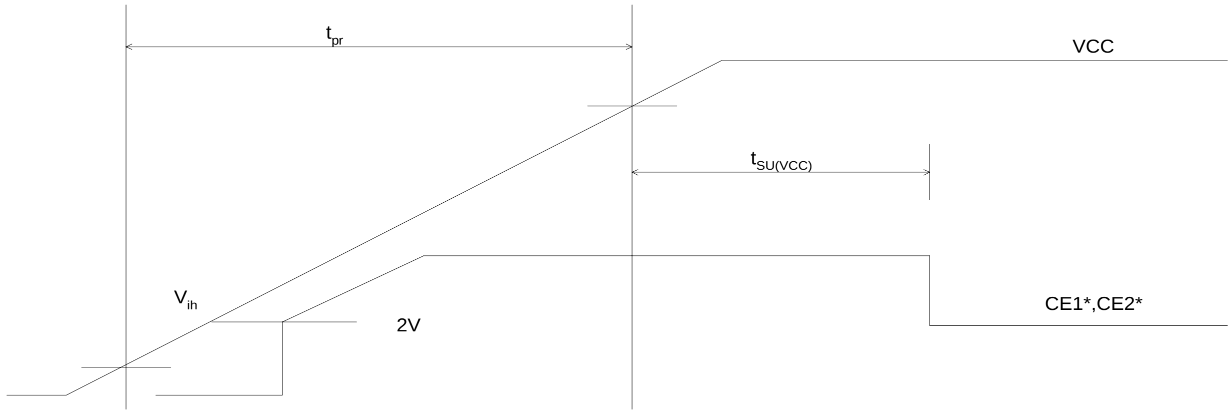


Figure 10: Power-up Timing Diagram

3.9.2 Power-down Timing Diagram

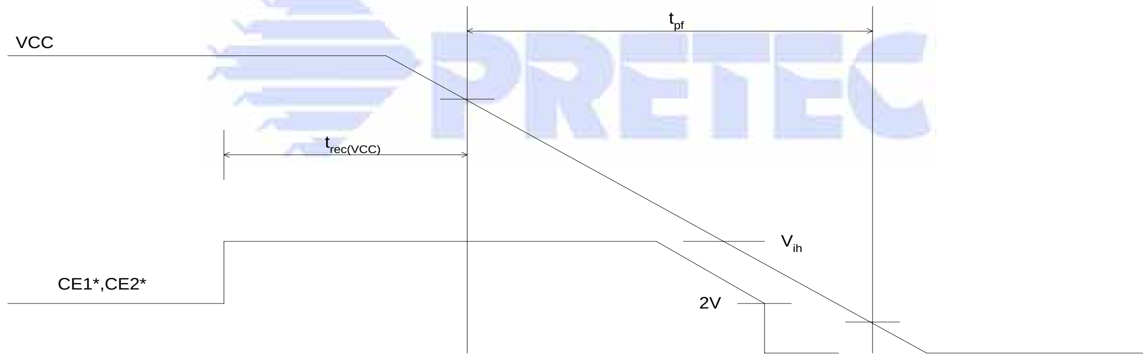
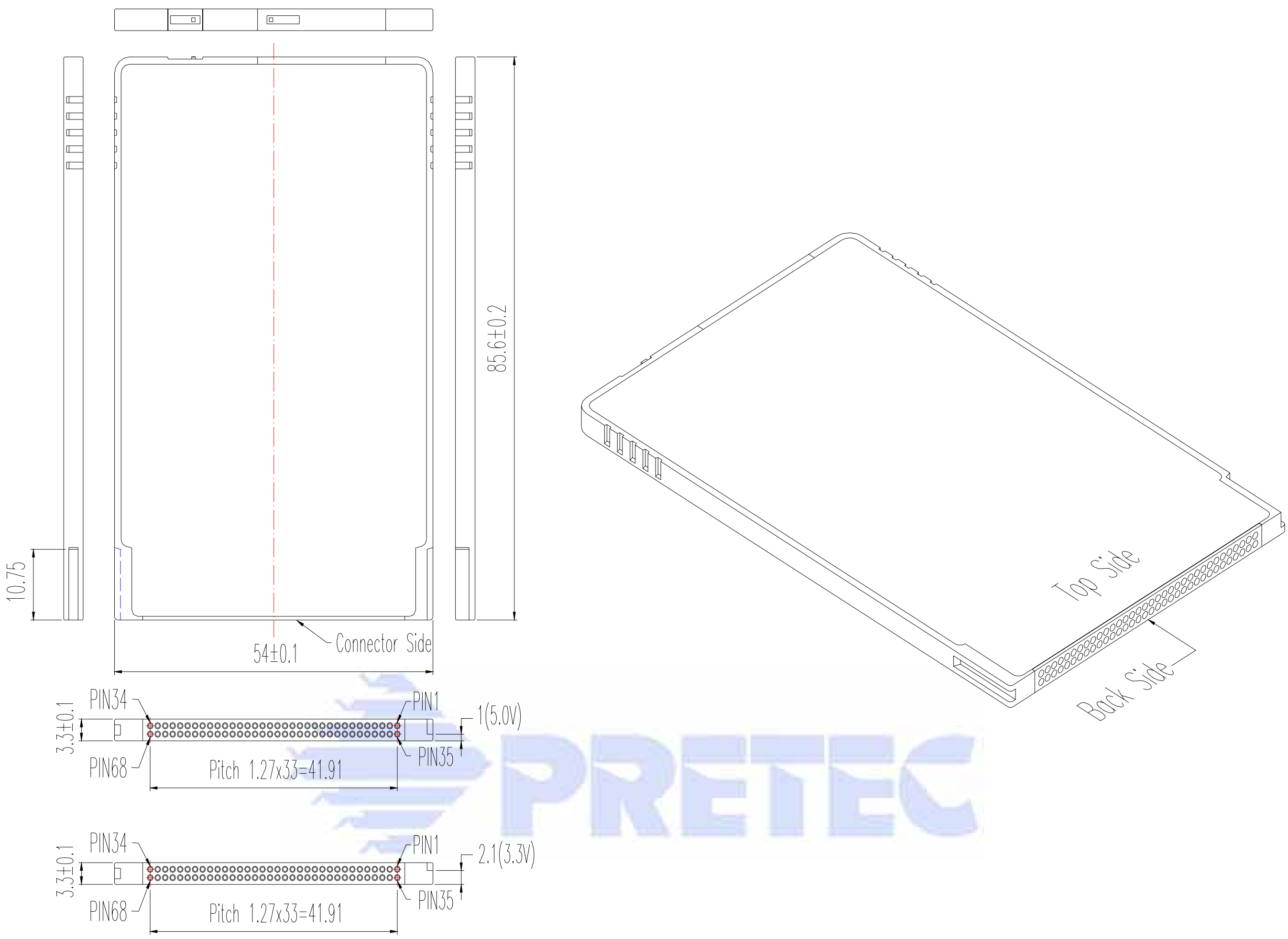


Figure 11: Power-down Timing Diagram

3.10 Outline Dimensions



(Unit: mm)

Figure 12: Outline dimensions of SRAM Card